Reg. No. : | | | | | | | | | | |

Question Paper Code: 43402

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. A(A+B) is same as

   (a) A (b) B (c) AB (d) A+AB

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The difference bit output of a half-subtractor is the same as

   (a) difference bit output of a full-subtractor
   (b) sum bit output of a half-adder
   (c) sum bit output of a full-adder
   (d) carry bit output of a half-adder

4. A device that convert from decimal to BCD is

   (a) decoder (b) encoder (c) multiplexer (d) demultiplexer

5. Which latch is called a transparent latch

   (a) SR latch (b) JK latch (c) D latch (d) T latch

6. How many flip-flops are needed for a 4-bit counter?

   (a) 2 (b) 3 (c) 4 (d) 6

7. The voltage needed for a TTL IC power supply is

(a) 5V dc (b) 10 V dc (c) 2 V dc (d) 20 V dc

8. Which of the following memories in non-volatile memory?

(a) ROM (b) PROM
(c) Ferrite core memory (d) None of these

9. Hazards occurs in

(a) Sequential circuit (b) Combinational circuit
(c) Both (a) and (b) (d) None of these

10. In synchronous sequential circuits, the memory elements are

(a) unclocked flip-flops (b) clocked flip-flops
(c) Both (a) and (b) (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Define Associative law and Distributive law.

12. Compare half adder & full adder.

13. Differentiate between Latch and Flip-flop.

14. Draw the circuit diagram of a TTL-NAND gate with totem pole output.

15. List the design procedure of Asynchronous sequential circuits.

PART - C (5 x 16 = 80 Marks)

16. (a) Realize the following function as Multilevel NAND –NAND gate and Multilevel NOR –NOR gate

$F = \bar{A} B + B (C + D) + E\bar{F} (\bar{B} + \bar{D})$ (16)

Or

(b) Consider the minimization of the following switching function using the QUINE-McCLUSKEY method. $F(x_1, x_2, x_3, x_4)=\sum(0, 5, 7, 8, 9, 10, 11, 14, 15)$. (16)

17. (a) (i) Construct the full adder using two half adders. (4)

(ii) Explain about the 4x1 multiplexer and Implement the function $F (A, B, C) = \sum(1, 3, 5, 6)$ using a multiplexer. (12)

Or

(b) With Truth table, design BCD-to-excess-3 code converter and obtain its logic diagram. (16)

18. (a) Explain synchronous decade counter using T flip flop. (16)

Or

(b) (i) Realize D flip-flop using SR flip-flop. (8)

(ii) With neat illustration explain in detail about 4-bit parallel-in-serial out shift register. (8)

19. (a) Briefly explain about PLD's with a suitable example. (16)

Or

(b) (i) Differentiate registered PAL and configurable PAL (8)

(ii) Design a 4-bit binary–to gray code converter using PROM. (8)

20. (a) Design a sequence detector circuit that produces an output 1 whenever the sequence 101101 is detected. (16)

Or

(b) Design serial binary adder using D-flip-flop. (16)

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