Reg. No. : | | | | | | | | | | |

Question Paper Code: 33402

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Obtain the *XS-3* code and 9's complement for $(428)_{10}$.
2. Find the complement of $A + BC + AB$.
3. Draw the logic diagram of a 4-bit adder- subtractor circuit.
4. What is data selector?
5. Mention the problems faced by ripple counter.
6. What is meant by Shift Register? List its types.
7. State the advantages and disadvantages of TTL.
8. Distinguish between PLA and PAL.
9. List the steps for the design of asynchronous sequential circuit.
10. Define flow table in Asynchronous Sequential circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Using k-map method, obtain the minimal SOP and POS expressions for the function. $f(x, y, z, w) = \sum m(1, 3, 4, 5, 6, 7, 9, 12, 13)$. (8)

(ii) Simplify the following expression using Boolean laws: (8)

$Y = (A + C)(A + D)(B + C)(B + D)$

$Y = (B + BC)(B + B'C)(B+D)$

Or

(b) Simplify the following function using tabulation method.

$f(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ (16)

12. (a) Design a 4 bit magnitude comparator using logic gates. (16)

Or

(b) Implement the following Boolean function using 16:1 multiplexer

$f(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$. (16)

13. (a) (i) Narrate the operating principle of master slave JK flip flop. (6)

(ii) Design a MOD-6 synchronous counter using J-K Flip-Flops. (10)

Or

(b) Design and draw a 3 bit synchronous counter which goes through the following states: $1 – 3 – 5 – 7 – 1$ (16)

14. (a) With neat diagram explain the RAM organization. (16)

Or

(b) Design a Two-Bit Magnitude Comparator with a PLA. (16)

15. (a) Narrate the different types of Hazards. Discuss in detail how the hazards can be eliminated. (16)

Or

(b) (i) Illustrate with an example the hierarchical modeling concepts used in Verilog HDL. (10)

(ii) Write a Verilog code to perform 4 bit Full Adder with carry look ahead. (6)