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Reg. No. : | | | | | | | | | | |

Question Paper Code: 56403

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Sixth Semester

Electronics and Communication Engineering

15UEC603- VLSI DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. The primary mechanisms for modeling the behavior of a Verilog design needs CO1- R

   (a) Initial statement (b) Always statement (c) Both (a) and (b) (d) Only (a)

2. In CMOS fabrication, the photoresist layer is exposed to CO2- R

   (a) visible light (b) infra red light (c) ultraviolet light (d) fluorescent

3. The number of pass transistors connected in series can be increased if CO3- R

   (a) Compressor is connected (b) Ground is connected

   (c) Voltage regulator is connected (d) Buffer is connected

4. In CMOS NAND gate, p transistors are connected in CO4- R

   (a) Series (b) Parallel (c) Cascade (d) Random

5. The process of removing equivalent faults is called as CO5- R

   (a) Equivalent removing (b) Fault collapsing

   (c) Fault reduction (d) Bulk damaging

PART – B (5 x 3= 15 Marks)

6. Mention the data types used in Verilog HDL. CO1- R

7. Why the tunneling current is higher for nMOS transistors than pMOS transistors with silicon gate? CO2- U

8.		Calculate logical effort and parasitic delay of n-input NOR gate.	CO3- Ana	
9.		Implement a 2:1 MUX using pass transistor.	CO4- Ana	
10.		Differentiate testers and test fixtures.	CO5- U	

PART – C (5 x 16= 80 Marks)

11.	(a)	(i) Write the Verilog description of 4-bit Ripple carry Adder at Gate level Abstraction.	CO1- App	(8)
		(ii) Write a program for 4-to-1 Multiplexer, Using Conditional Operators in dataflow level of abstraction in Verilog.	CO1- App	(8)
		Or		
	(b)	Give a gate level description of a 2-4 decoder circuit with relevant logic diagram and Verilog HDL source code.	CO1- App	(16)
12.	(a)	(i) With neat diagram explain the n-well and channel formation in CMOS process.	CO2- U	(8)
		(ii) Describe the CMOS inverter and derive its DC characteristics.	CO2- U	(8)
		Or		
	(b)	(i) How the influences of body effect varies the threshold voltage of MOS transistor and also derive the DC equations of drain – to – source current for three operating regions?	CO2- U	(8)
		(ii) Briefly discuss about the CMOS process enhancement and layout design rules.	CO2- U	(8)
13.	(a)	Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expression.	CO3- U	(16)
		Or		
	(b)	Derive the expressions for effective resistance and capacitance estimation using Elmore's RC delay model.	CO3- U	(16)
14.	(a)	(i) Implement an EX-OR gate using CMOS logic.	CO4- U	(6)
		(ii) Describe the principle of constant field scaling and constant voltage scaling and also write its effect on device characterization.	CO4- U	(10)
		Or		
	(b)	Explain the sequencing methods of Flip flops and latches.	CO4- U	(16)

15.	(a)	Explain briefly about Ad Hoc Testable Design Techniques.	CO5- U	(16)
		Or		
	(b)	(i) Draw and explain the BILBO	CO5- U	(8)
		(ii) Discuss in detail about silicon debug principle.	CO5- U	(8)

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