Reg. No. : | | | | | | | | | | |

Question Paper Code: 46404

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Sixth Semester

Electronics and Communication Engineering

14UEC604-VLSI DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(Smith chart may be permitted)

PART A - (10 x 1 = 10 Marks)

1. CMOS IC packages are available in

   (a) DIP configuration (b) SOIC configuration
   (c) DIP and SOIC configurations (d) Neither DIP nor SOIC configuration

2. _____ is ideally suited for applications using battery power or battery backup power.

   (a) MOS (b) P-MOS (c) N-MOS (d) CMOS

3. In accordance to the scaling technology , the total delay of the logic circuit depends on

   (a) The capacitor to be charged
   (b) The voltage through which capacitance must be charged
   (c) Available current
   (d) All of the above

4. In CMOS circuits, which type of power dissipation occurs due to switching of transient current & discharging of load capacitance?

(a) Static dissipation (b) Dynamic dissipation

(c) Both a and b (d) None of the above

5. The output of latches will remain in set/reset until

(a) The trigger pulse is given to change the state

(b) Any pulse given to go into previous state

(c) They don't get any pulse more

(d) None of the Mentioned

6. The sequential circuit is also called

(a) Flip-flop (b) Latch (c) Strobe (d) None of the Mentioned

7. Boundary scan test is used to test

(a) Pins (b) Multipliers (c) Boards (d) wires

8. CMOS domino logic occupies

(a) Smaller area (b) Larger area

(c) Both of the mentioned (d) None of the mentioned

9. In VHDL, which object/s is/are used to connect entities together for the model formation

(a) Constant (b) Variable (c) Signal (d) All the above

10. Among the VHDL features, which language statements are executed at the same time in parallel flow?

(a) Concurrent (b) Sequential (c) Net-list (d) Test-bench

PART - B (5 x 2 = 10 Marks)

11. Define threshold voltage in CMOS.

12. What is the fundamental goal in Device modeling?

13. State time borrowing.

14. What is stuck – at fault?

15. What is the structural gate-level modeling?

PART - C (5 x 16 = 80 Marks)

16. (a) Draw and explain the DC transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation. (16)

Or

(b) Explain in detail about region and modes of operations in MOSFET. (16)

17. (a) What are the various reliability problems associated with the failure of Integrated circuits? Explain elaborately with relevant diagrams. (16)

Or

(b) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (16)

18. (a) Describe the basic principles of operation of pseudo Nmos, Dynamic Cmos, domino and NP domino logic with neat diagrams. (16)

Or

(b) Explain in detail about sequencing dynamic circuits and synchronizers. (16)

19. (a) What are the various testing methods to be considered while designing a VLSI circuit? (16)

Or

(b) (i) Explain Ad-Hoc testing and Built in soft test techniques. (8)

(ii) What are the challenges involved in silicon debugging? Explain. (8)

20. (a) Write the verilog code in gate level modeling for multiplexer and D-latch. (16)

Or

(b) Explain the looping statements and procedural assignments in VERILOG HDL. (16)