Reg. No. : | | | | | | | | | | |

Question Paper Code: 36404

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is the purpose of design rule?
2. Define twin – well process? Why it is so called?
3. State the types of power dissipation.
4. What is meant by design margin?
5. State the reasons for the speed advantage of CVSL family.
6. State any two criteria for low power logic design.
7. What is the need for testing?
8. What is mean by logic verification?
9. Write a verilog module for a half adder.
10. What are gate primitives?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Discuss about the layout design rules. (8)

(ii) Demonstrate the different technology related CAD issues. (8)

Or

(b) Illustrate the DC transfer characteristics of a CMOS inverter. (16)

12. (a) What is a BSIM model? Give its versions with SPICE levels. Mention the features of BSIM model. (16)

Or

(b) Demonstrate the concept of device characterization in CMOS processes. (16)

13. (a) (i) Explain the issues related to the design of low power logic design. (8)

(ii) In short explain about static CMOS design. (8)

Or

(b) (i) Discuss about the conventional CMOS flip flops. (8)

(ii) Summarize the sequencing of dynamic circuits. (8)

14. (a) Describe in detail, the various manufacturing test principles in CMOS testing. (16)

Or

(b) Explain the method of boundary scan test in detail. (16)

15. (a) Develop a Verilog code for 4 – bit comparator using behavioral modeling. (16)

Or

(b) Explain behavioral and gate level modeling with suitable example. (16)