Reg. No.:					

Question Paper Code: 44423

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Fourth Semester

Computer Science and Engineering

14UEC423 - MICROPROCESSORS AND MICROCONTROLLERS

(Common to Information Technology)

(Regulation 2014)							
Du	ration: Three hours			Maximum: 100 Marks			
		Answer AI	LL Questions				
		PART A - (10	x 1 = 10 Marks)				
1.	SUB B instruction in	n 8085 microprocesso	r				
	(b) sets the zero(c) sets the zero		result				
2.	2. Vector address of interrupt RST 7.5 is						
	(a) 0.002CH	(b) 0.002CH	(c) 0.003CH	(d) none of these			
3.	In 8086 each segme	nemory.					
	(a) 8	(b) 16	(c)32	(d) 64			
4.	4. Which of the following instruction is a logical instruction?						
	(a) DIV AB	(b) TEST	(c) CALL	(d) AAM			
5.	The 8087 coprocess instruction	sor operate in	with an 8086 p.	rocessor and with the same			

(a) series, byte(c) series, bits

(b) parallel, byte

(d) parallel, bits

The synchronization bet	ween processo	or and coprocessor can be	e done by		
(a) RQ/GT ₀ and RQ/0	GT ₁ , FWAIT				
How many address lines	are required to	access 1 MB RAM using	microprocessor?		
(a) 16	(b) 8	(c) 20	(d) 12		
The 8279 is a					
(a) DMA controller(c) counter		(b) programmable keybo(d) interrupt controller	oard display interface		
What will be the output a MOV A, #55 ANL A, #67	fter execution	of the following instruction	on?		
(a) 54	(b) 45	(c) 55	(d) 67		
What will be the output a MOV A, #55 ANL A, #67	fter execution	of the following instruction	on?		
(a) 54	(b) 45	(c) 55	(d) 67		
	PART - B ($(5 \times 2 = 10 \text{ Marks})$			
Classify the signals of 80	85.				
List out the flags present	in 8086.				
Compare closely coupled	and loosely c	oupled configurations of c	o-processor.		
Highlight the method use memory at high speed.	d to transfer la	arge blocks of data between	n external device and		
Draw the format of PSW	of 8051.				
	PART - C (5 x 16 = 80 Marks)			
(a) Draw and explain the		,	(16)		
· · · · · · · · · · · · · · · · · · ·		•	(-0)		
(b) Explain the instruction	n set of 8085		(16)		
	(a) RQ/GT ₀ and RQ/G (c) BUSY and TEST, How many address lines at (a) 16 The 8279 is a (a) DMA controller (c) counter What will be the output at MOV A, #55 ANL A, #67 (a) 54 What will be the output at MOV A, #55 ANL A, #67 (a) 54 Classify the signals of 80 List out the flags present at Compare closely coupled Highlight the method use memory at high speed. Draw the format of PSW	connection and the	(c) BUSY and TEST, FWAIT How many address lines are required to access 1 MB RAM using (a) 16 (b) 8 (c) 20 The 8279 is a (a) DMA controller (b) programmable keyber (c) counter (d) interrupt controller What will be the output after execution of the following instruction MOV A, #55 ANL A, #67 (a) 54 (b) 45 (c) 55 What will be the output after execution of the following instruction MOV A, #55 ANL A, #67 (a) 54 (b) 45 (c) 55 PART - B (5 x 2 = 10 Marks) Classify the signals of 8085. List out the flags present in 8086. Compare closely coupled and loosely coupled configurations of compare thigh speed.		

17.	(a)	(i) Illustrate the each pins of 8086 with neat explanation.	(8)
		(ii) Outline about the MACRO with example.	(8)
		Or	
	(b)	Explain in detail about Interrupt Service Routine (ISR) of 8086 processor.	(16)
18.	(a)	Draw the architecture of 8087 numeric data processor and explain each block.	(16)
		Or	
	(b)	Explain the architecture of 8089 I/O processor with a diagram.	(16)
19.	(a)	Show the function of keyboard and display controller with a neat sketch.	(16)
		Or	
	(b)	Describe the block diagram of IC 8237 DMA controller.	(16)
20.	(a)	Show the block diagram of 8051 microcontroller and explain the functions in o	detail (16)
		Or	
	(b)	Explain the interfacing of ADC and DAC with 8051 microcontroller.	(16)