Reg. No. : | | | | | | | | | | |

Question Paper Code: 39403

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Discuss the stored program concept.
2. List out the register level circuit components.
3. Point out the advantages of Co-processors.
4. Compare spatial expansion and temporal expansion.
5. What is microprogramming?
6. What is Write-After-Write (WAW) hazard?
7. Compare sequential access and random access memories.
8. Define memory latency.
9. What is memory mapped I/O?
10. What is non-maskable interrupt? Write the action performed on receipt of a NMI?

PART - B (5 x 16 = 80 Marks)

11. (a) Briefly explain the organization of CPU and memory of the IAS computer with instruction set. (16)

Or

(b) Explain the operation of each functional unit in the computer system with suitable diagram. (16)

12. (a) (i) With example illustrate the principle and working of binary multiplication used in computers. (8)

(ii) Write the significance and basic idea of pipeline processing. (8)

Or

(b) With a neat sketch, explain in detail about logic design for fast adders. (16)

13. (a) (i) Explain the various issues in data path implementation. (10)

(ii) Compare horizontal and vertical organization of architecture design. (6)

Or

(b) (i) Describe the design details of pipelined processing. (10)

(ii) Write short notes on Nano programming. (6)

14. (a) Give the structures of semiconductor RAM memories. (16)

Or

(b) Explain the concepts of memory hierarchies. (16)

15. (a) List out the three bus arbitration schemes. Explain any two with a diagram. (16)

Or

(b) (i) With a diagram explain static and dynamic redundancy for designing fault tolerant system. (10)

(ii) Compare RISC and CISC processor. (6)