Question Paper Code: 53504

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Electronics and Instrumentation Engineering

15UEI304 - DIGITAL ELECTRONICS

(Regulation 2015)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Which of the following is the most widely used alphanumeric code for computer input and output?

    (a) Gray   (b) ASCII   (c) Parity   (d) EBCDIC

2. The Boolean algebra is mostly based on

    (a) Boolean theorem   (b) De Morgan's theorem
    (c) De Morpans theorem   (d) Standard theorem

3. How many entries will be in the truth table of a 3 input NAND gate?

    (a) 3   (b) 6   (c) 8   (d) 9

4. How many bits are required to store one BCD digit?

    (a) 1   (b) 2   (c) 3   (d) 4

5. For which of the following flip-flops, the output is clearly defined for all combinations of two inputs

    (a) Q type flip-flop   (b) R-S flip-lop   (c) J-K flip-lop   (d) D flip-flop

6. What is the difference between a ring shift counter and a Johnson shift counter?

    (a) there is no difference   (b) a ring is faster
    (c) the feedback is reversed   (d) the Johnson is faster

7. Which hazard is overcome by properly designed two level AND-OR or OR-AND circuit

    (a) dynamic hazard   (b) static-0 hazard

    (c) static-1 hazard   (d) none of the above

8. Which one is the suitable to detecting the hazard in circuit?

    (a) Logic gates   (b) Karnaugh map

    (c) Boolean expression   (d) None of these

9. Which of the following memories uses one transistor and one capacitor as basic memory unit

    (a) SRAM   (b) DRAM   (c) Both (a) and (b)   (d) none

10. In a read-only memory information can be stored

    (a) at the time of fabrication

    (b) by the user only once during its life time

    (c) by the user a number of times

    (d) in any of the above ways depending upon the type of memory

PART - B (5 x 2 = 10 Marks)

11. Convert 0.640625 decimal numbers to its octal equivalent.

12. Implement the Boolean Expression for EX – OR gate using NAND Gates.

13. What is edge-triggered flip-flop?

14. Mention the significance of state assignment.

15. What is programmable logic array? How it differs from ROM?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Convert the binary number $(101111.1101)_2$ in to decimal.   (8)

        (ii) Design a 4 bit BCD to Excess-3 code converter.   (8)

Or

    (b) Simplify the following expression using K-map

        (i) $Y = \sum_m (7, 9, 10, 11, 12, 13, 14, 15)$

        (ii) $Y = m_1 + m_5 + m_{10} + m_{11} + m_{12} + m_{13} + m_{15}$ (16)

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17. (a) (i) Examine about the formation of inverter using CMOS and its operation. (8)

(ii) Identify the TTL logic circuit for a 3-input NAND gate with appropriate explanation. (8)

Or

(b) (i) Give the CMOS logic circuit for NOR gate and explain its operation. (8)

(ii) Explain the TTL circuit output connections. (8)

18. (a) (i) Explain the triggering of flip flops. (8)

(ii) Draw the logic diagram of master slave JK flip flop. (8)

Or

(b) Explain the operation of universal shift register with logic diagram. (16)

19. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X. (16)

Or

(b) What are hazards? When does the hazard occur in combinational circuits and quote an example? Name the types of hazards and how they are avoided. (16)

20. (a) Explain the classification of memories. (16)

Or

(b) (i) Draw the block diagram of a PLA and explain its IC 7575-PLA. (16)

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