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**Question Paper Code: 43506** 

## B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Electronics and Instrumentation Engineering

## 14UEI306 - DIGITAL ELECTRONICS

(Regulation 2014)

	(Tto Salatio	11 201 1)				
	Duration: Three hours	N	Iaximum: 100 Marks			
	Answer ALL	Questions				
	PART A - (10 x 1	1 = 10 Marks)				
1.	The three basic logic gates are					
	<ul><li>(a) AND,OR and NOT gate</li><li>(c) NAND, OR and NOT</li></ul>		<ul><li>(b) AND,OR and NOR</li><li>(d) None of the above</li></ul>			
2.	Each square in a karnaugh map represents a					
	(a) Points (b) Values	(c) Minterm	(d) Maxterm			
3.	A comparator is a special combinational relative magnitude of numbers	-	rily to compare the			
	(a) two decimal (b) three decimal	(c) two binary	(d) three binary			
4.	A comparator is a special combinational relative magnitude of numbers	• •	rily to compare the			
	(a) two decimal (b) three decimal	(c) two binary	(d) three binary			

5. How is a J-K flip-flop made to toggle?					
(a) $J = 0$ , $K = 0$	(b) $J = 1$ , $K = 0$	(c) $J = 0$ , $K = 1$	(d) $J = 1$ , $K = 1$		
What is a major disa	dvantage of RAM?				
(a) Its access spo	eed is too slow	(b) Its matrix size is too big			
(c) It is volatile		(d) High power consumption			
In positive logic,					
(a) a $HIGH = 1$ ,	a $LOW = 0$	(b) a LOW = $1$ , a HIGH = $0$			
(c) only HIGHs	are present	(d) only LOW	s are present		
For JK flip flop with	J=1, K=0, the output a	after clock pulse will be			
(a) 0	(b) 1	(c) High Impedance	(d) No change		
PAL consists of a pro	grammable array	and a fixed array	with output logic.		
(a) NAND and I	NOR	(b) AND and NO	R		
(c) NAND and (	OR	(d) AND and OR			
. What is an OTP dev	ice?				
(a) Optical transporting port		(b) Octal transmitting pixel			
(c) Operational	topical portable	(d) One-time program	mable		
	PART - B (5 x	2 = 10 Marks)			
. What are called don	't care conditions?				
Define Multiplexer	and draw its block diag	ram.			
. List out the applicat	ions of Flip Flops.				
Define Glitch.					
	(a) J = 0, K = 0  What is a major disa  (a) Its access spece (c) It is volatile  In positive logic,  (a) a HIGH = 1,  (c) only HIGHs  For JK flip flop with (a) 0  PAL consists of a product of the control of the	(a) J = 0, K = 0  What is a major disadvantage of RAM?  (a) Its access speed is too slow (c) It is volatile  In positive logic,  (a) a HIGH = 1, a LOW = 0 (c) only HIGHs are present  For JK flip flop with J=1, K=0, the output a (a) 0  (b) 1  PAL consists of a programmable array (a) NAND and NOR (c) NAND and OR  What is an OTP device?  (a) Optical transporting port (c) Operational topical portable  PART - B (5 x  What are called don't care conditions?  Define Multiplexer and draw its block diag  List out the applications of Flip Flops.	(a) J = 0, K = 0  What is a major disadvantage of RAM?  (a) Its access speed is too slow (b) Its matrix (c) It is volatile  (d) High power  In positive logic,  (a) a HIGH = 1, a LOW = 0 (b) a LOW = 0 (c) only HIGHs are present  (d) only LOW  For JK flip flop with J=1, K=0, the output after clock pulse will be a low a programmable array and a fixed array  (a) NAND and NOR (b) AND and NOR (c) NAND and OR  (d) AND and OR  What is an OTP device?  (a) Optical transporting port (b) Octal transmitting (c) Operational topical portable  (d) One-time program  PART - B (5 x 2 = 10 Marks)  What are called don't care conditions?  Define Multiplexer and draw its block diagram.		

PART - C (5 x 16 = 80 Marks)

15. What is meant by PLA?

16.	(a)	Minimize the logic function $Y(A,B,C,D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$ . Karnaugh map. Draw logic circuit for the simplified function.	. Use (16)
		Or	
17.		Simplify the Boolean function using tabulation method. $Y(A, B, C, D) = \sum m (1, 2, 3, 5, 9, 12, 14, 15) + \sum D (4, 8, 11)$ . Draw the block schematic of Magnitude Comparator and explain its operations.	(16) (16)
		Or	
	(b)	Design BCD adder and explain its working with necessary circuits.	(16)
18.	(a)	Sketch a 4-bit serial in serial out shift register and draw its waveforms.	(16)
		Or	
	(b)	Explain the operation universal shift register with logic diagram.	(16)
19.	(a)	Design an Asynchronous circuit that has two inputs $x_1$ and $x_2$ and output z. The circuit is required to give an output whenever the input sequence $(0,0)$ $(0,1)$ and $(1,1)$ received but only in that order.	
		Or	
	(b)	Explain the different methods of state assignment.	(16)
20.	(a)	Explain about RAM and its types.	(16)
		Or	
	(b)	Explain with neat diagrams a RAM architecture.	(16)