Reg. No. : | | | | | | | | | | |

Question Paper Code: 47504

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Seventh Semester

Electronics and Instrumentation Engineering

14UEI704 - VLSI SYSTEM DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The limitations of scaling are

   (a) Broad channel effects (b) narrow channel effects

   (c) interference effects (d) none of the above

2. The advantages of CMOS technology is

   (a) Low input impedance (b) high input impedance

   (c) high noise margin (d) low noise margin

3. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____ region

   (a) Linear (b) Saturation (c) Non saturation (d) Non saturation

4. In basic inverter circuit, _____ is connected to ground

   (a) Source (b) Gates (c) Drain (d) Resistance

5. In dynamic CMOS logic _____ is used

   (a) Two phase clock (b) Three phase clock

   (c) One phase clock (d) Four phase clock

6. Which multiplier is very well suited for twos complement numebers?

(a) Baugh-wooley algorithm (b) Wallace trees

(c) Dadda multipliers (d) Modified booth encoding

7. PAL has

(a) Programmable AND array and a fixed OR array

(b) Programmable OR array and a fixed AND array

(c) Programmable AND and OR array

(d) All the above

8. Which type of device FPGA are?

(a) SLD (b) SROM (c) EPROM (d) PLD back

9. What do VHDL stand for?

(a) Verilog hardware description language (b) VHSIC hardware description language

(c) very hardware description language (d) VMEbus description language

10. Among the VHDL features ,which language statements are executed at the same time in parallel flow CO5- R

(a) concurrent (b) sequentia (c) net-list (d) test bench

PART - B (5 x 2 = 10 Marks)

11. What is depletion mode operation MOS?

12. What is stick diagram? What are the uses of stick diagram?

13. What is a multiplier circuit?

14. What is programmable logic array?

15. Give the classification of operators used in VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) Explain about nMOS Transistor with neat diagram. (16)

Or

(b) Explain in detail about the scaling concept of MOS Transistor (16)

17. (a) Explain about DC Characteristics of CMOS inverter circuit with neat diagram. (16)

Or

(b) Explain in detail about the Stick Diagram and layout diagram. (16)

18.(a) Discuss in detail about the Dynamic CMOS design. (16)

Or

(b) Explain multiplication with an example and discuss the types of multipliers. (16)

19. (a) Explain in detail about FPGA Interconnecting Procedure. (16)

Or

(b) Explain in detail about Floor planning, Routing &Placement. (16)

20. (a) Write VHDL testbench code for 4:1 multiplexer. (16)

Or

(b) Write VHDL program for Half adder & Full adder. (16)

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