Reg. No. : | | | | | | | | | | |

Question Paper Code: 37504

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Seventh Semester

Electronics and Instrumentation Engineering

01UEI704 - VLSI SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What are the second order effects in a MOS Transistor?
2. What are the advantages of Twin-tub process?
3. Define short channel devices.
4. Indicate the different symbols used for various regions in stick diagram.
5. Draw the CMOS implementation of 4-to-1 MUX using transmission gates.
6. What are the advantages of AOI implementation of two level logic functions?
7. What are the advantages of PLA?
8. Mention some of PLDs.
9. What are the different design units in VHDL?
10. What is the use of block statements in VHDL?

PART - B (5 x 16 = 80 Marks)

11. (a) Elaborate the process and steps involved in CMOS Fabrication of VLSI system technology. (16)

Or

(b) Explain the operation of MOS transistor in depletion mode and enhancement mode. (16)

12. (a) Draw the CMOS inverter transfer characteristics and explain its operation, clearly indicating the various regions. (16)

Or

(b) Derive the expression for 4:1 and 8:1 pull up and pull down ratios of nMOS inverter. (16)

13. (a) Explain with neat diagrams the design of 4:1 multiplexer using dynamic CMOS and Domino logic. (16)

Or

(b) (i) Construct an AOI CMOS equivalent for the sum of products expression Y= ABC+ADE+EFG. (16)

14. (a) Explain the general architecture of FPGA and bring about different programmable blocks used. (16)

Or

(b) (i) Explain the architecture of any one type of FPGA. (8)

(ii) Write short notes on floor planning and placement. (8)

15. (a) (i) Explain a simple test bench for any one Flip-Flop with necessary VHDL code. (8)

(ii) Write the structural VHDL code for 5-bit synchronous counter. (8)

Or

(b) Write the VHDL code for Finite State Machine using behavioral and structural modeling. (16)