A **Reg. No. :** | | | | | | | | | | |

Question Paper Code: 59501

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Elective

Electronics and Instrumentation Engineering

15UEI901– VLSI SYSTEM DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. In MOS transistors, _____ is used for their gates. CO1- R

   (a) Metal (b) Polysilicon (c) Silicon-di-Oxide (d) Gallium

2. The photoresist layer is exposed to CO1- R

   (a) Visible Light (b) Infra Red Light (c) Ultraviolet Light (d) LED

3. Which color is used for n-diffusion? CO2- R

   (a) Red (b) Blue (c) Yellow (d) Green

4. The transistors used in BiCMOS are: CO2- R

   (a) BJT (b) MOSFET (c) Both BJT and MOSFETs (d) JFET

5. In clocked CMOS logic, output in evaluated in CO3- R

   (a) On Period (b) Off Period (c) Both Periods (d) Half of On Period

6. The output of the circuit only depends on the present inputs is CO3- R

   (a) Sequential (b) Combinational (c) Combined (d) Single circuits

7. PLA contains CO4- R

   (a) AND and OR arrays (b) NAND and OR arrays

   (c) NOT and AND arrays (d) NOR and OR arrays

8. PIP in XILINIX means CO4- R

(a) Picture in Picture (b) Programmable interconnect point

(c) programmable interface point (d) None of above

9. The members function of VHDL modules declared between CO5- R

(a) BEGIN – END (b) { - }

(c) { - } (d) (-)

10. The full form of VHDL is CO5- R

(a)Very High Descriptive Language

(b)Very High Definition Language

(c)Variable Definition Language

(d) None of the Mentioned

PART – B (5 x 2= 10Marks)

11. Define body effect. CO1- U

12. Mention techniques to reduce switching activity. CO2- R

13. Define Contamination delay. CO3- R

14. List the steps used for design flow in VLSI. CO4 -R

15. What is subprogram? CO5- U

PART – C (5 x 16= 80Marks)

16. (a) (i) Explain with neat diagrams the fabrication process of n-well CMOS transistor. CO1- U (8)

(ii) Describe the operation of CMOS Inverter. CO1- U (8)

Or

(b) Explain the different steps involved in the fabrication of NMOS with a neat diagram. CO1- U (16)

17. (a) Determine the pull up to pull-down ratio of nMOS Inverter driven by another nMOS Inverter. CO2- App (16)

Or

(b) Discuss the principles of constant field and lateral scaling. .Write the effects of the above scaling methods on the device characteristics. CO2- Ana (16)

18. (a) Explain the domino and dual rail domino logic families with neat diagram. CO3- U (16)

Or

(b) (i) Design an 4 x 4 Barrel Shifter and explain its operation. CO3- Ana (8)

(ii) Design a 4 x 1 Multiplexer using CMOS static pull up device CO3- Ana (8)

19. (a) Design and sketch the stick diagram of a NMOS NOR-NOR PLA realization of the product lines with three output lines. CO4- U (16)

$P_0 = \overline{I_0}\,\overline{I_1}$ $P_1 = \overline{I_0} I_1$ $P_2 = I_0 I_1 \overline{I_2}$ $P_3 = I_0 I_2$

$Y_0 = P_1$ $Y_1 = P_0 + P_2 + P_3$ $Y_2 = P_1 + P_2$

Or

(b) Explain about building block architecture of FPGA. CO4- U (16)

20. (a) Write the VHDL program to design encoder and decoder circuits. CO5- U (16)

Or

(b) (i)Write a testbench VHDL program for NAND gate. CO5- App (8)

(ii)Draw the diagram of down counter and write the VHDL program. CO5- App (8)