Reg. No. : | | | | | | | | | | |

Question Paper Code: 43203

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Computer Science and Engineering

14UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(Smith chart may be permitted)

PART A - (10 x 1 = 10 Marks)

1. The time between the start and completion of a task is referred to as

   (a) response time (b) execution time (c) throughput (d) both a and b

2. The range of a n-bit 2's complement representation of a number is

   (a) -2^{n-1} to $2^{n-1} - 1$ (b) -2^{n} to $2^{n-1} - 1$ (c) -2^{n-1} to $2^{n} - 1$ (d) -2^{n-1} to 2^{n}

3. Arithmetic Logic Unit (ALU) is used to perform

   (a) addition (b) left shift (c) right shift (d) all of these

4. The number of bits for exponent field in double precision floating point number is

   (a) 8 bits (b) 11 bits (c) 20 bits (d) 23 bits

5. The throughput of an ideal pipeline with *k* stages is _____ instruction/clock cycle

   (a) *k* (b) *k*-1 (c) 1 (d) 2

6. The registers, the ALU, and the interconnecting bus are collectively referredto as the _____

(a) Datapath (b) Subpath
(c) Connecting path (d) None of these

7. Multithreading an interactive program will increase responsiveness to the user by

(a) continuing to run even if a part of it is blocked
(b) waiting for one part to finish before the other begins
(c) asking the user to decide the order of multithreading
(d) None of these

8. In a multithreaded environment _____

(a) Each thread is allocated with new memory from main memory
(b) Main thread terminates after the termination of child threads
(c) Every process can have only one thread
(d) No termination

9. The extra time needed to bring the data into memory in case of a miss is called as _____

(a) Delay (b) Propagation time (c) Miss penalty (d) Data latency

10. The signal sent to the device from the processor to the device after receiving an Interrupt is

(a) Interrupt-acknowledge (b) Return signal
(c) Service signal (d) Permission signal

PART - B (5 x 2 = 10 Marks)

11. What is meant by spilling registers?

12. Give the overflow conditions for addition and subtraction.

13. List the five steps to be followed for executing MIPS instructions.

14. Provide Flynn's classification of parallel computers.

15. Find the average memory access time for a processor with a 1 *ns* clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction and cache access time of 1 clock cycle.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Explain the basic components of a computer system. (10)

(ii) Consider the following 32-bit MIPS instructions

```
lw   r8, 1200(r9)
add  r8, r18, r8
sw   r8, 1200(r9)
```

What is the MIPS machine language code for these three instructions? Note that the opcodes of lw, add and sw are 35, 0 and 43 respectively. (6)

Or

(b) (i) Describe the different classes of Instruction format with examples. (12)

(ii) Registers *R*1 and *R*2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions?

Load 20(*R*1), *R*5

Add –(*R*2), *R*5 (4)

17. (a) (i) Explain the rules for basic arithmetic operations of floating point numbers? (8)

(ii) Explain Guard bit and Truncation? (8)

Or

(b) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. (16)

18. (a) Explain briefly the operation of a simple data path with control unit with neat diagram. (16)

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome / minimize these hazards? (16)

19. (a) Explain the concept of instruction level parallelism in detail. (16)

Or

(b) Explain Flynn's classification of computers. (16)

20. (a) (i) What is bus arbitration? Describe the centralized approach for bus arbitration with help of diagram. (8)

(ii) Explain the need for memory hierarchy technology, with a four-level of memory. (8)

Or

(b) (i) What is DMA? What are the steps in DMA transfer? (8)

(ii) Explain the working of a DMA controller with a diagram. (8)