Reg. No. : | | | | | | | | | | |

Question Paper Code: 33203

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2018

Third Semester

Computer Science and Engineering

01UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is memory access time? What is the typical range of memory access time for modern RAM units?
2. Differentiate logical operations and control operations.
3. State the truth table of 2 bit binary adder.
4. List the features of booth multiplication algorithm.
5. What is meant by Data path?
6. What is operand forwarding? When it is used?
7. Give an example for WAW Hazard.
8. What is instruction level parallelism?
9. Define TLB hit and Miss.
10. What is meant by bus arbitration?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Write short notes on branching and condition codes. (8)

(ii) With suitable example, explain the addition of signed numbers. (8)

Or

(b) Write in detail about various addressing modes. (16)

12. (a) Illustrate the multiplication algorithm in detail. (16)

Or

(b) Explain the floating point addition steps and algorithm in detail. (16)

13. (a) What is instruction hazard? Explain the methods for dealing with the instruction hazards. (16)

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. (16)

14. (a) Explain concept of instruction level parallelism in detail. Discuss about the challenges. (16)

Or

(b) Explain how performance efficiency is achieved by Multicore Processors. (16)

15. (a) Explain the different ways used for improving the cache performance. (16)

Or

(b) How does a virtual address get translated into physical address? Explain in detail with the neat diagram. Explain the use of TLB. (16)