Reg. No. : | | | | | | | | | | |

Question Paper Code: 32207

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Second Semester

Computer Science and Engineering

01UCS207- DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Which gates are called as the universal gates? What are their advantages?
2. Convert $(25.35)_{10}$ into its octal equivalent.
3. State the importance of tabulation method?
4. What do you mean by comparator?
5. Define HDL.
6. Determine the number of address lines required for accessing 2MB and a 64KB memory.
7. Show how a JK flip flop can be operated as a toggle flip flop.
8. State the differences between combinational logic and sequential logic.
9. What is a critical race? State its importance in an asynchronous sequential circuit.
10. List the assumptions that must be made for a fundamental mode circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Simplify the following Boolean expression.

$$Y = \overline{\overline{A\overline{B}} + ABC} + A\,(B + A\overline{B})$$ (8)

(ii) Simplify the following boolean function using K-map method.

$F\,(A,B,C,D,E) = \sum m\,(1,5,7,13,14,15,17,18,21,22,25,29) + \sum d\,(6,9,19,23,30)$ (8)

Or

(b) Minimize the expression using Quine McCluskey method (Tabulation) method $F=\sum m(0, 1,9, 15, 24, 29, 30)+\sum d(8, 11, 31)$. (16)

12. (a) Explain the different type of binary codes with suitable examples. (16)

Or

(b) (i) Design a combinational logic circuit to compare two 2-bit binary numbers A and B and to check whether A<B, A=B or A>B. (8)

(ii) Explain the BCD adder with a neat block diagram. (8)

13. (a) (i) Implement the function, $F\,(A,B,C,D) = \sum m\,(0,1,2,5,6,9,12,14)$ using two 4x1 multiplexers. (8)

(ii) Write a structural Verilog description for a 2x4 decoder with a neat sketch. (8)

Or

(b) Implement the Boolean function using 8:1 multiplexer

$F(A, B, C, D) = AB'D + A'C'D + B'CD' + AC'D$. (16)

14. (a) With suitable examples explain state reduction and state assignment of sequential circuits. (16)

Or

(b) (i) Explain in detail about parallel in serial out shift register, with neat sketches. (10)

(ii) Write the HDL for full adder circuits. (6)

15. (a) Explain the various static and dynamic hazards in digital circuits. Give the hazard free realization of the following Boolean expression.

$F(I, J, K, L) = \sum_m(1, 3, 4, 5, 6, 7, 9, 11, 15)$. (16)

Or

(b) Explain the method for the minimization of primitive flow table with an example. (16)